CLAIMS

What is claimed is:

1 A semiconductor device comprising:

a row of transistors each having a stack gate structure and a drain;

a layer of type-2 polysilicon interconnecting the transistors in the row; and

a source region adjacent to the layer of type-2 polysilicon having a contact and a N-type junction extending across the source region that provides a planar electrical path between the drains of the transistors and the contact, thereby reducing resistance of the source region.

2 The semiconductor of claim 1 wherein the transistors are located in core regions and isolation regions between pairs of adjacent transistors comprise respective P-type regions

3 The semiconductor of claim 1 wherein the transistors are located over active areas in the substrate, and the active areas include N-type regions.

4 A method for fabricating a semiconductor device having a planar source region, the method comprising the steps of:

(a) patterning stack gate transistors in active areas of a substrate, wherein

the transistors include a layer of poly1 and a layer of poly2 and have a drain;

(b) isolating adjacent columns of transistors with P-type regions in the substrate; and

(c) providing a source region adjacent to a row of transistors that has a continuous N-type junction for forming a planar electrical connection between the drains of the transistors in the row and a source region contact.

5 The method of claim 4 wherein steps (a) and (b) further include the steps of:

(i) defining active areas and isolation areas in a substrate;

(ii) performing a core Vt implant;

(iii) depositing tunnel oxide over the substrate;

(iv) patterning layer of Poly1 over the substrate to form columns of Poly1 over the active areas;

(v) performing a P-type isolation implant using the Poly1 as the mask to create P-type isolation regions;

(vi) depositing a layer of oxide nitride over the substrate; and

(vii) performing a Poly2 deposition and stack gate mask and etch.

6 The method of claim 4 wherein step (c) further includes the steps of:

(i) patterning a source/drain mask with openings for a N-type implant;

(ii) performing a N-type implant to form N-type regions under the active areas;

(iii) patterning a Vss implant mask for a Vss implant in a source region; and

(iv) performing the Vss implant in the source region to overcompensate the P-type isolation regions into N-type regions to create a continuous N-type junction in the source region, and thereby forming a planar source region with improved resistance.

7 A method for fabricating a planar transistor, the method comprising the steps of:

(a) defining active areas and isolation areas in a substrate;

(b) performing a core Vt implant;

(c) depositing tunnel oxide over the substrate;

(d) patterning layer of Poly1 over the substrate to form columns of Poly1 over the active areas;

(e) performing a P-type isolation implant using the Poly1 as the mask to create P-type isolation regions;

(f) depositing a layer of oxide nitride over the substrate;

(g) performing a Poly2 deposition and stack gate mask and etch;

(h) patterning a source/drain mask with openings for a N-type implant;

(i) performing a N-type implant to form N-type regions under the active areas;

(j) patterning a Vss implant mask for a Vss implant in a source region; and

(k) performing the Vss implant in the source region to overcompensate the P-type isolation regions into N-type regions to create a continuous N-type junction in the source region, and thereby forming a planar source region with improved resistance.

8 The method of claim 7 wherein step (e) further includes the step of: providing the P-type implant at a higher doping level than that for the core of Vt implant.

9 The method of claim 7 wherein step (e) further includes the step of: if a Poly1 hard mask is used performing the P-type isolation implant after the Poly1 hard mask is patterned.

10 The method of claim 7 wherein step (e) further includes the step of: if a Poly1 spacer and etched is performed, performing the P-type isolation after the Poly1 spacer and etch.